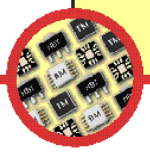
GaAs MMIC Power Amplifier



DESCRIPTION

AMCOM's AM003536WM-BM/FM-R is an ultra broadband GaAs MMIC power amplifier. It has 23dB gain and 36dBm output power over the 0.01 to 3.5GHz band. This MMIC is in a ceramic package with both RF and DC leads at the lower level of the package to facilitate low-cost SMT assembly to the PC board. When mounting directly to PCB, please see application note AN700 for instructions. Because of high DC power dissipation, we strongly recommend to mount these devices directly on a metal heat sink. The AM003536WM-FM-R is the AM003536WM-BM-R mounted on a gold plated copper flange carrier. There are two screw holes on the flange to facilitate screwing on to a metal heat sink. This MMIC is RoHS compliant.

FEATURES

- Wide bandwidth from 10MHz to 3.5GHz
- High output power, P1dB = 36dBm
- High gain, 23dB
- Input /Output matched to 50 Ohms

APPLICATIONS

- Software Radio
- Instrumentation
- Gain block

TYPICAL PERFORMANCE * (Bias Conditions**: V_{dd} = +20V, I_{dq1} = 150mA, I_{dq2} = 550mA)

Parameters	Minimum	Typical **	Maximum
Frequency	0.02 – 2.5GHz	0.01 – 3.5GHz	
Small Signal Gain	20dB	23dB	26dB
Gain Ripple		± 1.5dB	± 3.0dB
P1dB @ 1GHz	33.0dBm	35.0dBm	
Psat	35.0dBm	37.0dBm	
Efficiency @ P1dB		20%	
IP3 @ 1GHz		48dBm	
Input Return Loss	13dB	20dB	
Output Return Loss	7dB	10dB	
Thermal Resistance		4.5°C/W	

* Specifications subject to change without notice.

** Gate biases corresponding to above currents are V_{gs1}=-1V, I_{gs1} < 2mA, V_{gs2}=-0.75V, I_{gs2} < 5mA and may vary from lot to lot. Gate currents could reach above limits only near power saturation.

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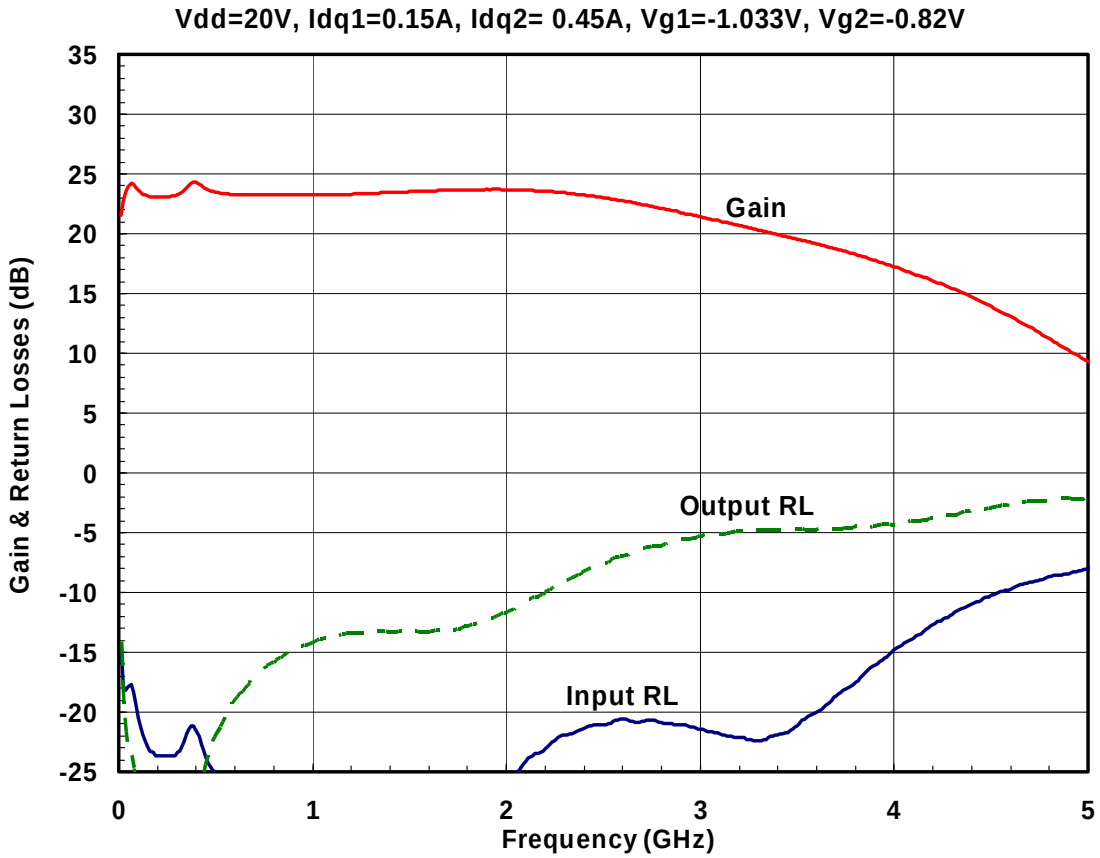
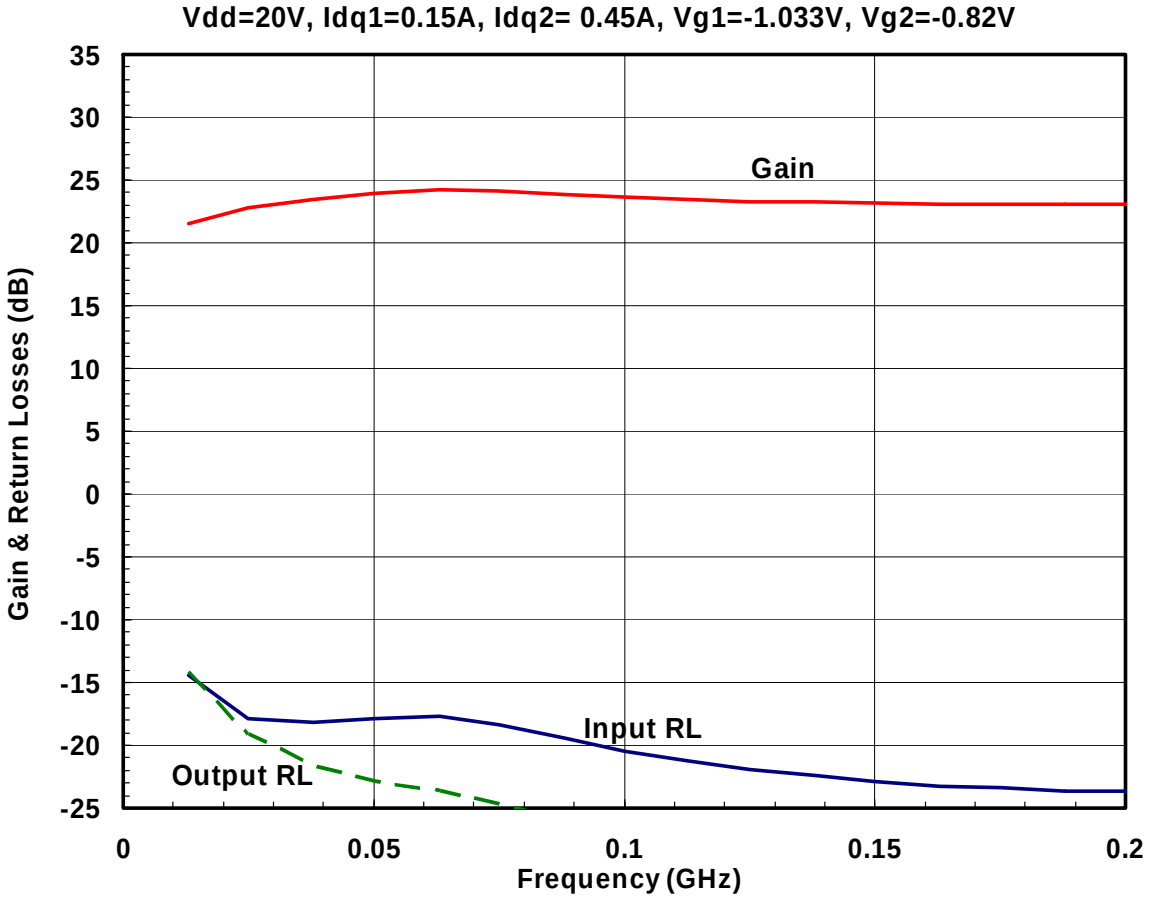
ABSOLUTE MAXIMUM RATING

Parameters	Symbol	Rating
Drain source voltage	V_{dd}	24V
Gate source voltage	V_{gs1} & V_{gs2}	-3V
Drain source current	I_{dq1}	0.17A
Drain source current	I_{dq2}	0.60A
Continuous dissipation at 25ºC	P_t	18W
Channel temperature	T_{ch}	175°C
Operating temperature	T_{op}	-55°C to +85°C
Storage temperature	T_{sto}	-55°C to +135°C

SMALL SIGNAL MEASUREMENTS*

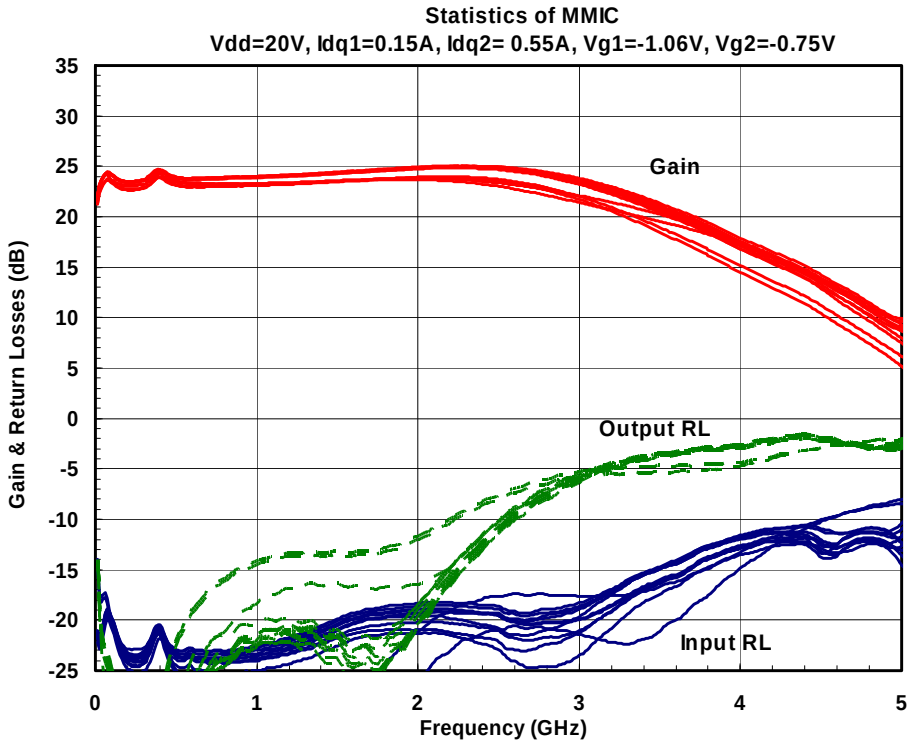


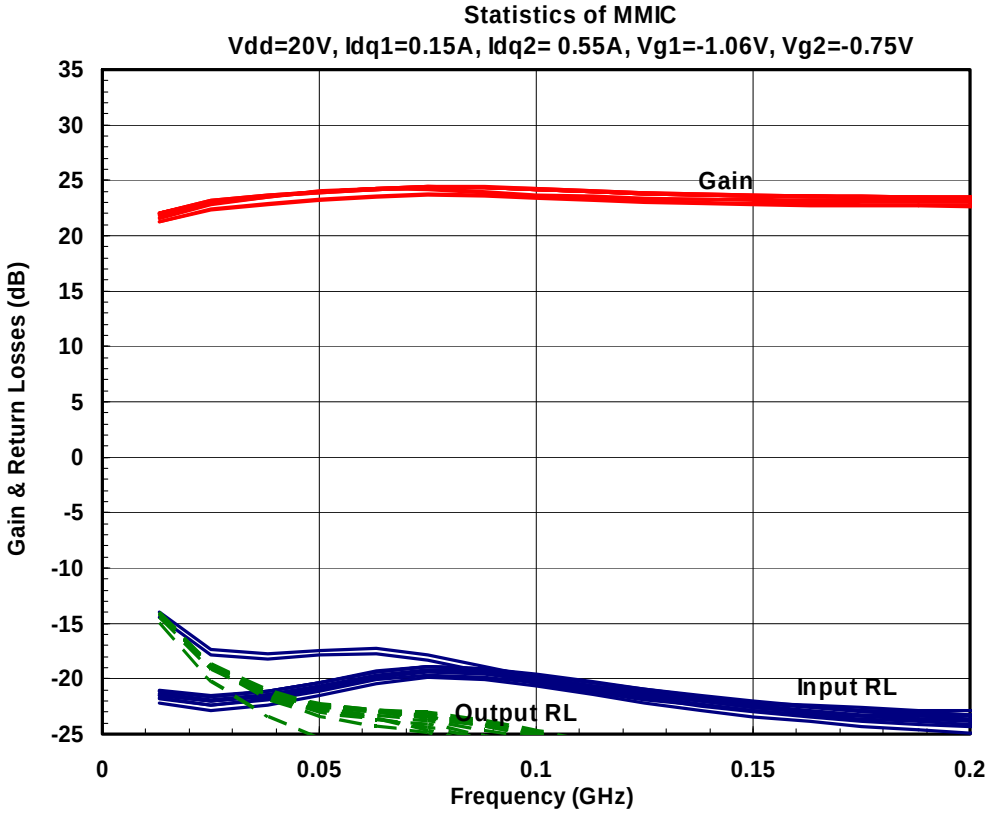
EXTENDED LOW FREQUENCY SCALE



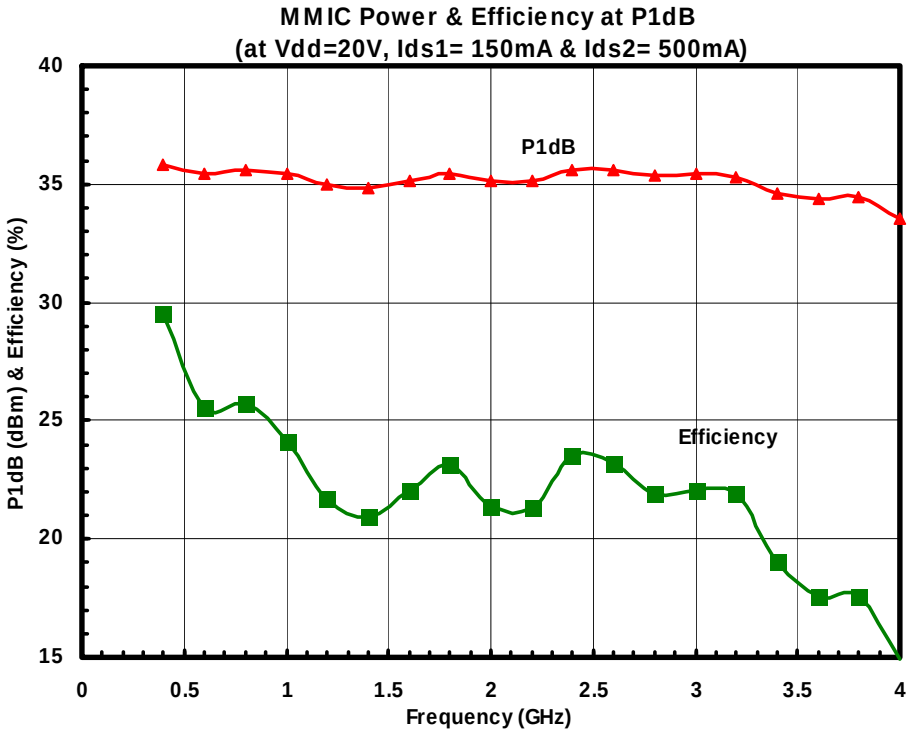
* S-Parameters measured using bias tee at the output. MMIC could be operated at lower than V_{dd}=+20V with almost same small signal parameters. V_{gs1} & V_{gs2} vary with V_{dd} and may need slight adjustments.

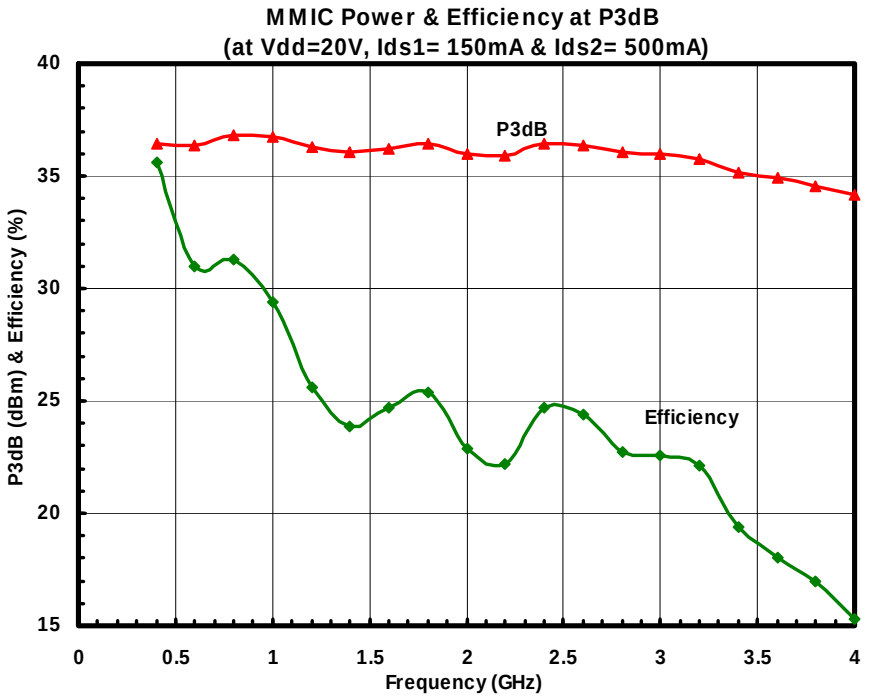
SMALL SIGNAL STATISTICS



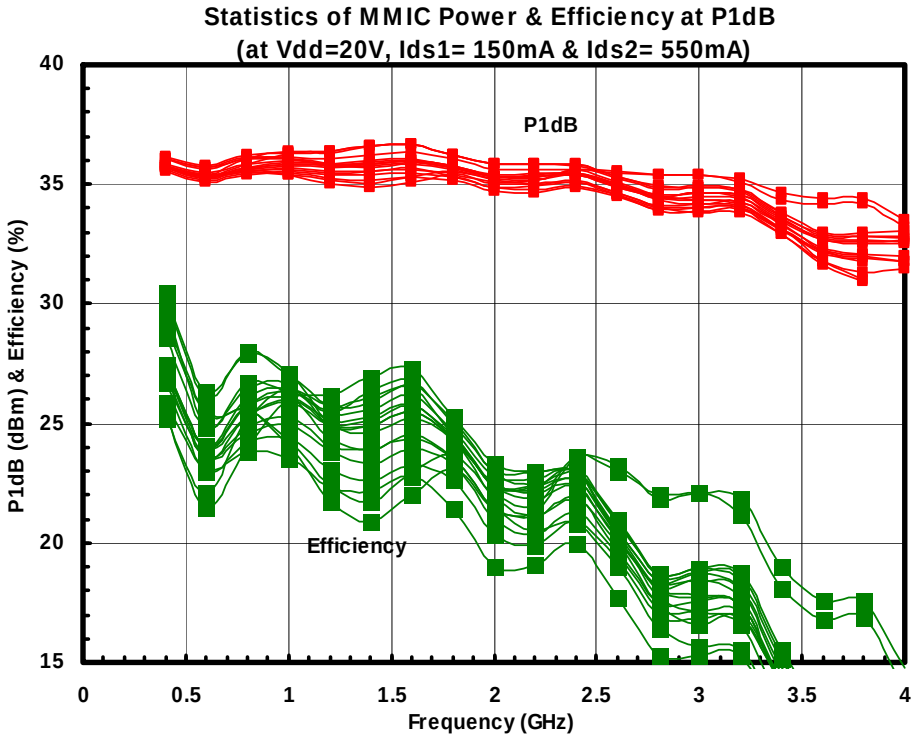


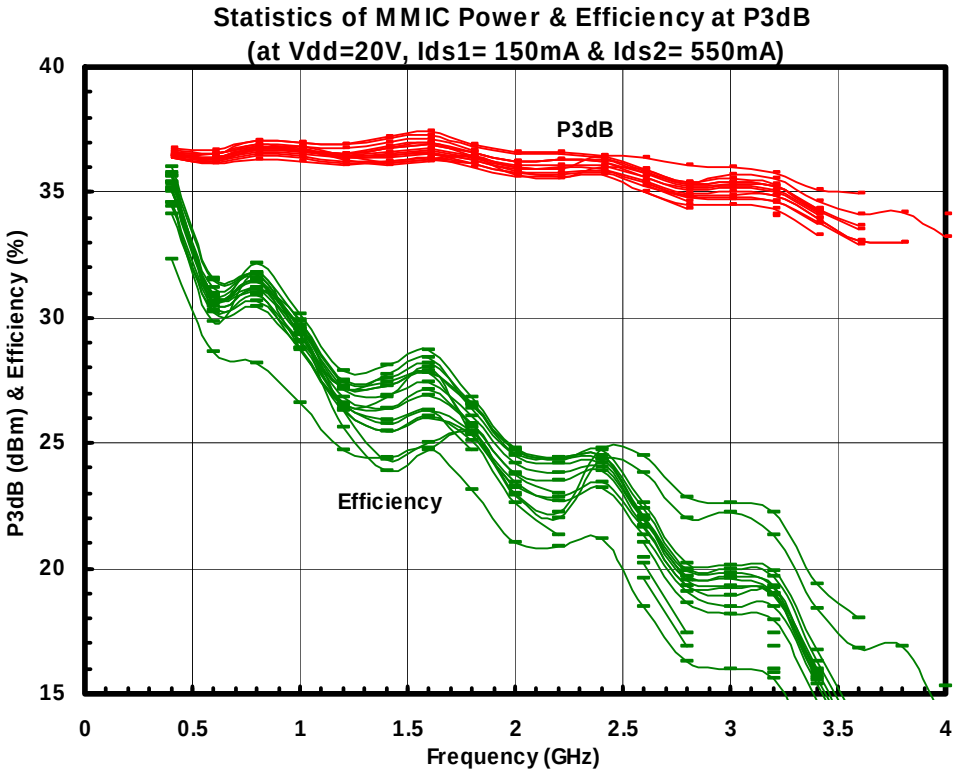
POWER DATA*



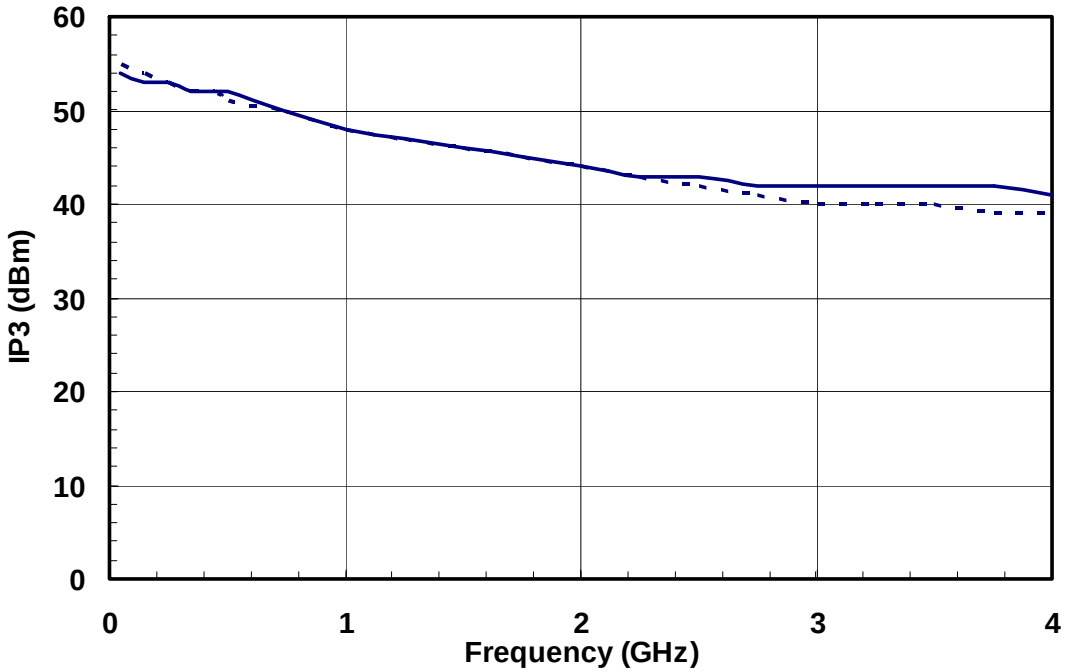


* Power measured using bias tee at the output. MMIC could be operated at lower than V_{dd}=+20V with reduced power output. V_{gs1} & V_{gs2} vary with V_{dd} and may need slight adjustments.

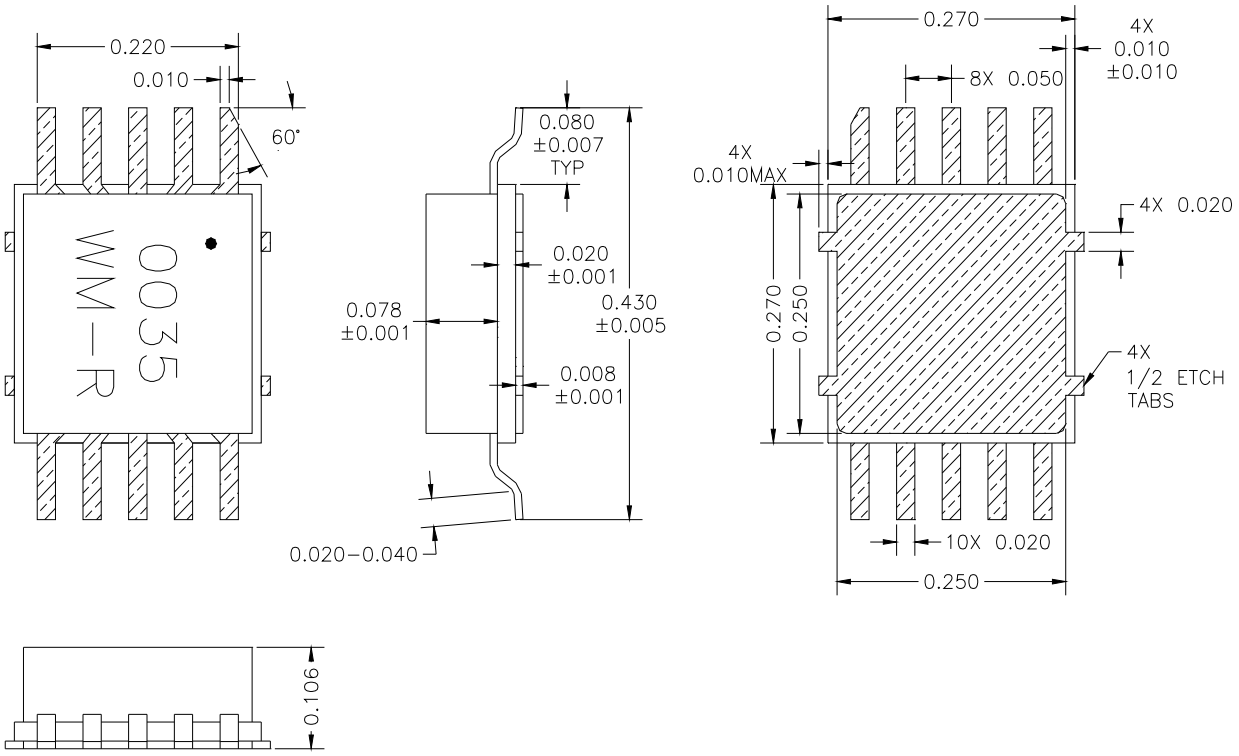

Statistics of MMIC Power & Efficiency at P1dB
(at Vdd=20V, Ids1= 150mA & Ids2= 550mA)
P1dB
Efficiency
P1dB (dBm) & Efficiency (%)
Frequency (GHz)
40
35
30
25
20
15
0
0.5
1
1.5
2
2.5
3
3.5
4


Statistics of MMIC Power & Efficiency at P3dB
(at Vdd=20V, Ids1= 150mA & Ids2= 550mA)
P3dB
Efficiency
P3dB (dBm) & Efficiency (%)
Frequency (GHz)
40
35
30
25
20
15
0
0.5
1
1.5
2
2.5
3
3.5
4

IP3 as a function of Frequency

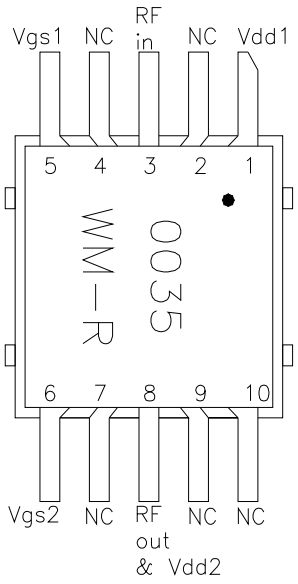


PACKAGE OUTLINE (BM)



* Gate biases are for reference only and may vary from lot to lot.

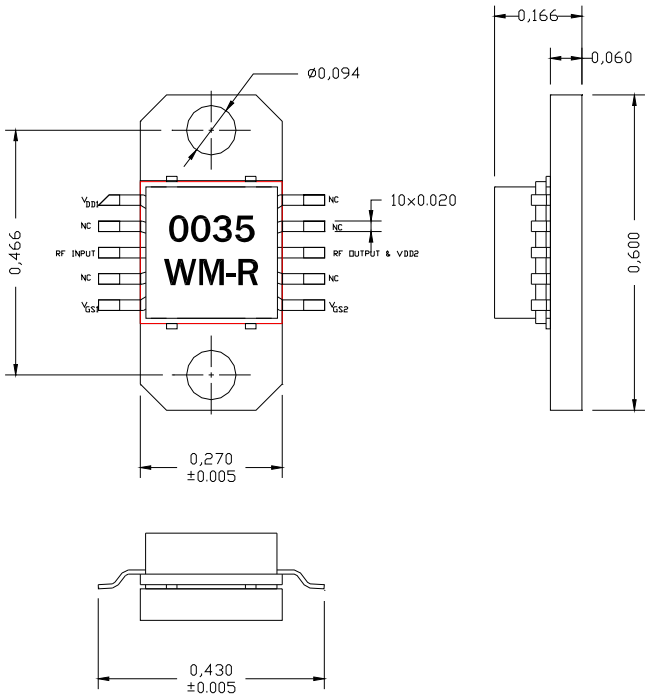
PIN LAYOUT



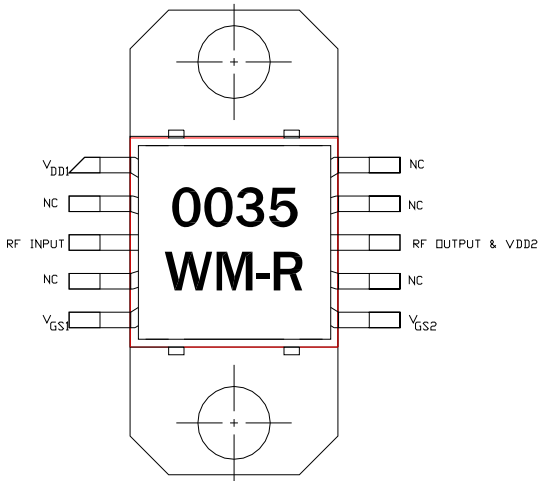
Pin No.	Function	Bias
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.0V
6	Vgs2	-0.75V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* Gate voltage may vary from lot to lot

PACKAGE OUTLINE (FM)



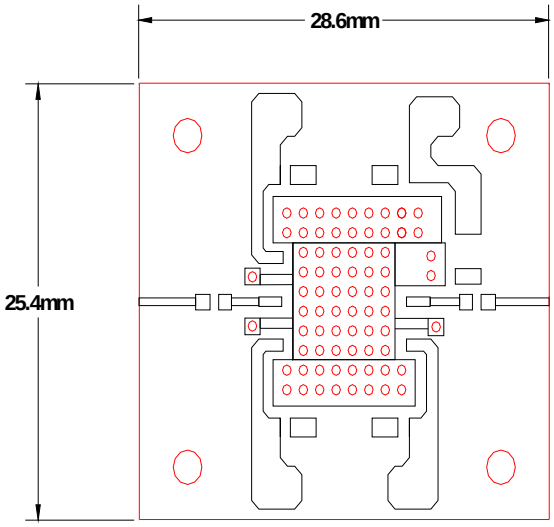
PIN LAYOUT

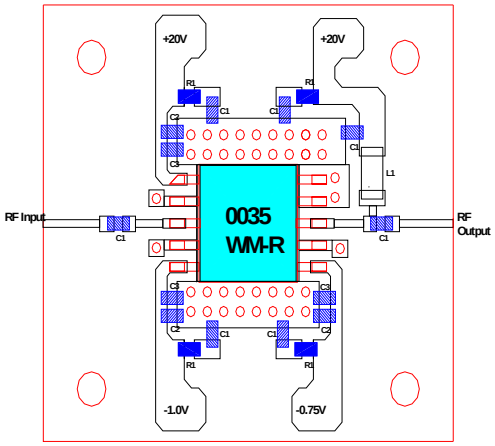


Pin No.	Function	Bias
1	Vdd1	+20V
2	NC	
3	RF in	
4	NC	
5	Vgs1	-1.0V
6	Vgs2	-0.75V
7	NC	
8	RF out & Vdd2	+20V
9	NC	
10	NC	

* Gate voltage may vary from lot to lot

TEST CIRCUIT for BM Package





Notes:
1- Material is 10mils FR4 with 1 Oz Copper
2- All vias are plated thru
(min. via thickness = 25um)
3- R1=50 Ohms, R2=0 Ohms,
C1=1000pF, C2=100pF, C3=20pF, L1=300nH

Resistor
Capacitor

Important Notes:

1- The +20V Bias to the output port could be provided via a bias tee or suitable chokes to be soldered on the board. Inductance of choke should be large enough to have high impedance at lowest frequency of operation (300nH is adequate).

2- Recommended current biases are 150mA and 500mA for the first stage and second stage respectively. Gate biases are for reference only. At V_{dd1} & V_{dd2} = +20V, V_{gs1} & V_{gs2} values are -1.0V and -0.75V respectively to obtain these desired currents. V_{gs1} & V_{gs2} could be adjusted to vary the currents going thru the first stage (V_{dd1} pin) and the second stage (V_{dd2} pin) respectively.

3- Do not apply V_{dd1} & V_{dd2} without proper negative voltages on V_{gs1} & V_{gs2}.

4- The currents flowing out of the V_{gs1} & V_{gs2} pins are less than 2mA & 5mA respectively at P_{1dB}.

5- External 1 µF dipped tantalum capacitor should be attached to Vd and Vg to decouple external bias leads.